What is claimed is:

1. A stacked gate flash memory cell, comprising:

a substrate having a cell trench and two adjacent isolation trenches therein, the cell trench having two substrate sides and two isolation sides contacting the adjacent isolation trenches, the isolation trench having two substrate sides and one cell side contacting the adjacent cell trench;

a bottom insulating layer disposed on the bottom of the cell trench;

a pair of tunnel oxide layers, each disposed on the substrate side of the cell trench and the bottom insulating layer;

a pair of floating gates, each disposed on the substrate side of the cell trench and covering the tunnel oxide layer;

a conformal inter-gate dielectric layer overlying the tunnel oxide layers and the bottom insulating layer;

a control gate overlying the inter-gate dielectric layer in the cell trench; and

two pairs of source/drain regions, each respectively disposed on the same substrate side of each isolation trench.

2. The cell as claimed in claim 1, wherein the substrate is a P-type silicon substrate.

3. The cell as claimed in claim 1, wherein the bottom insulating layer is silicon dioxide.

4. The cell as claimed in claim 1, wherein the tunnel oxide layer is silicon dioxide.

5. The cell as claimed in claim 1, wherein the floating gate and the control gate are N-type dopant doped polysilicon.

6. The cell as claimed in claim 1, wherein the inter-gate dielectric layer is silicon dioxide.

7. The cell as claimed in claim 1, wherein the isolation trench is filled with an insulating material comprising silicon dioxide.